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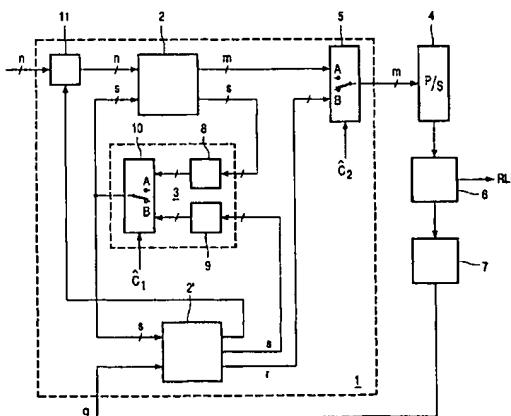
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- (71) Applicant: **KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]**; Groenewoudseweg 1, NL-5621 BA Bindhoven (NL).
- (72) Inventors: **KAHLMAN, Josephus, A., H., M.**; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **SCHOUHAMER**
- (74) Agent: **DEGUELLE, Wilhelmus, H., G.**; International Octrooibureau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).
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(54) Title: DEVICE FOR ENCODING A STREAM OF DATABITS OF A BINARY SOURCE SIGNAL INTO A STREAM OF DATABITS OF A BINARY CHANNEL SIGNAL, MEMORY MEANS, DEVICE FOR RECORDING INFORMATION, RECORD CARRIER, DEVICE FOR CODING AND DEVICE FOR PLAYING BACK



WO 01/95495 A1

(57) Abstract: In a device for encoding a stream of databits of a binary source signal into a stream of databits of a binary channel signal the bitstream of the source signal is divided into n-bit source words. The device comprises converting means adapted to convert a block of p consecutive n-bit source words into a corresponding block of p consecutive m-bit channel words, such that the conversion for at least most of the n-bit source words is parity preserving and/or parity inverting, where $m > n \geq 1$. The converting means comprise memory means which contain for each n-bit source word a number of m-bit channel words, arranged in coding states, and a corresponding state number, indicating the state for a next m-bit channel word. After each block of source words q dc-control sourcebits are added, which are converted into r dc-control channelbits, independent of the conversion of a following source word.

Device for encoding a stream of databits of a binary source signal into a stream of databits of a binary channel signal, memory means, device for recording information, record carrier, device for coding and device for playing back

The present invention relates to a device for encoding a stream of databits of a binary source signal into a stream of databits of a binary channel signal, wherein the bitstream of the source signal is divided into n-bit source words, which device comprises

converting means adapted to convert a block of p consecutive n-bit source words into a

- 5 corresponding block of p consecutive m-bit channel words, where p, n, m are integers and $m > n \geq 1$, the converting means comprising memory means which contain for each n-bit source word a number of m-bit channel words, arranged in coding states, and a corresponding state number, indicating the memory location for a next m-bit channel word.

Such a device is known from WO97/09718/A1 and describes a recording and
10 reproducing system, provided with a memory, which, in response to n-bit source words and respective table numbers, generates m-bit channel words and state numbers for next source word conversions. The conversions are not parity preserving. Further said known device comprises a selection circuit, which, in response to the m-bit channel words, calculates the running DSV (digital sum value) and provides for selection signals which indicate whether
15 the read out channel words have to increase or decrease the DSV. Although by these measures the dc-level may be incidentally reduced, an overall dc-suppression is not guaranteed, with the consequence that still distortions may be introduced in communicating systems which cannot handle a dc-component, as well as distortions in any recording of data on respective carriers.

20 In order to obtain a required dc-suppression, dc-control bits can be introduced on source level, however, with the consequence that the channel words do not correspond with the source words any longer. This means that, when there is an error on a data carrier, error propagation during reproducing may occur.

Further, in practice several encoding systems are known, e.g. in CD-recording
25 and reproducing systems EFM-encoding of 8-bit source words into 17-bit channel words is applied. During recording the encoded channel words are recorded on a data carrier, while during reproducing the channel words are decoded inversely. In DVD-recording and reproducing systems EFM-plus-encoding of 8-bit source words into 16-bit channel words is

applied. The channel signals therein are realized in a (2,10) sequence. However, in all these known systems a dc-suppression in the channel word sequence is not guaranteed.

Referring to the above it may be noticed that encoding devices in general provide for encoded channel words in a (d,k) sequence, wherein d is the number of 'zeros' which at least is present between two subsequent 'ones' in the serial datastream of the channel signal and k the number of 'zeros' which at most is present between two subsequent 'ones' in the serial datastream of the channel signal. The description in said international patent application shows a conversion of blocks of 8-bit source words into blocks of 15-bit channel words in a (2,14) sequence. Although, by the presence in the memory of several coding tables, the sequence of channel words obeys the d,k-constraints, a dc-suppression, as already mentioned, is not guaranteed, because the separate conversions of n-bit source words into m-bit channel words are not parity preserving.

The purpose of the invention is to obtain an encoding device as described in the opening paragraph in which a dc-suppression in the channel word sequence is guaranteed and in which, when there is an error on a data carrier, error propagation during reproducing is avoided.

Therefore, in a first embodiment according to the invention, the device as described in the opening paragraph is characterized in that the conversion for at least most of the n-bit source words is parity preserving and/or parity inverting and that after each block of source words q dc-control sourcebits are added, which dc-control sourcebits are converted into r dc-control channelbits. In a second embodiment according to the invention, the device is characterized in that the conversion for at least most of the n-bit source words is parity preserving and/or parity inverting and that after each block of source words q dc-control sourcebits are added, which dc-control sourcebits together with only a following n-bit source word is converted into a (r+m)-bit channelword, where q and r are integers. In both cases all the source words correspond with respective channel words; in other words, source words and channel words are permanently aligned with each other. By this measure error propagation will be avoided. As in the second embodiment a separate table is provided for the conversion of (n+q)-bit source words into (m+r)-bit channel words, which is more complicated than a simple table for the conversion of q-bit dc-control source bits into r dc-control channel bits, the first embodiment is preferred.

Although parity preserving codes are known per se, instead of a parity preserving conversion of source words into channel words, also a parity inverting conversion may be applied. The conversion is parity preserving when, if the number of 'ones' in a source

word is even, the number of 'ones' in a corresponding channel word is even too, and, if the number of 'ones' in a source word is odd, the number of 'ones' in a corresponding channel words is odd too. The conversion is parity inverting when, if the number of 'ones' in a source word is even, the number of 'ones' in a corresponding channel word is odd, and, if the number 5 of 'ones' in a source words is odd, the number of 'ones' in a corresponding channel words is even. In both cases the insertion of a dc-control bit provides for parity conversion

In both embodiments the channel output signal sequence supplied by the converting means may be fed to a precoder to determine a RLL (run length limited) output signal, which signal is supplied to a control signal generator to derive the dc-control bits.

10 Such a feedback loop for a parity preserving code is described in e.g. US-A-5,477,222, wherein between successive groups of p consecutive n-bit source words parity preserving bits are inserted in such a way that channel words obtained thereafter do not correspond with source words any longer and propagation errors may occur.

Like source word-to-channel word conversions, the dc-control source bits-to-15 dc-control channel bits conversion will depend on the last m-bit channel word, determining the state of the dc-control channel bits. Therefore, according to the invention the memory means further contain for each q dc-control source bits and for each state number r dc-control channel bits and a corresponding state number, indicating the memory location for a next m-bit channel word .

20 In a practical embodiment n=8, m=15, q=1 and r=2, while p may be chosen dependent on the desired dc-suppression. With a conversion rate 8/15 each source byte will correspond to a 15-bit channelword in one of the tables in the memory means, independently of the dc-control bits inserted.

When in a (d,k) channel word sequence in said practical embodiment d=2 and, 25 for example a source code in the preferred embodiment ends with "1", the dc-control bits will always be "00" as the next channel word may start with "1" and at least two zero's must be present between two "1's". This means that the control bits itself have no influence with respect to parity control. Therefore, in order to realize a parity control in this case and in suchlike cases, according to the invention, the device comprises inverting means, which, 30 depending on a last preceding channelword and on the dc-control channelbits, provides for inversion of an odd number of bits of a following source word; i.e. the inversion of 1, 3, 5, bits of a following source word. Such an inversion identifies dc-control source bit-to-dc control channel bit conversions with dc-control channel bits of the same parity, when the

following channel word is chosen from another coding state belonging to a respective source word.

As the various coding states in the memory means contain multiple used channel words, errors on a data carrier may occur, such that the source words to which the 5 channel words refer during reproducing, are not unambiguously determined. Therefore, according to the invention, the channel words in the coding states refer substantially to a same source word.

The invention further relates to memory means with a coding table for application in a device described above. According to the invention, the coding state may 10 contain 15-bit channel words to generate a parity preserving (2,14) sequence, or a parity preserving (2,13) sequence and even a (2,12) sequence. Although, in the latter case the k-constraint is further diminished, the disadvantage that only a small number of the 1024 source-to-channel conversions is not parity preserving must be accepted.

The invention also relates to a device for recording information, which device 15 comprises an encoding device according as described before for converting a series of channel words representing the information into a modulated signal and means for recording an information pattern corresponding to said modulated signal on a record carrier. Apart from the specific encoding device, the recording device can be the same as described in the above mentioned WO97/09718/A1, the content of which document must be considered as inserted 20 in the present specification.

The invention further relates to a record carrier on which a modulated signal is recorded, said signal comprising a series of channel words, obtained by encoding source words as described above.

Further, the invention relates to a device for decoding channel words into 25 source words comprising converting means with memory means containing the same coding states as the memory means in the encoding device according to the invention; however, the coding states now are read out inversely. In connection therewith the invention also relates to a device for playing back the information on said record carrier comprising a reading arrangement for reading said record carrier and a decoding device mentioned above.

30

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment described hereinafter and illustrated in the accompanying drawing. In the drawing:

Fig. 1 shows blockschematically an encoding device according to the invention;

Fig. 2 shows a dc-control source bit-to- dc-control channel bit conversion table;

5 Figs. 3A-3H show the coding states for a (2,14) parity preserving channel signal sequence;

Fig. 4A-4H show the coding states for a (2,13) parity preserving channel signal sequence; and

10 Fig. 5A-5H show the coding states for a (2, 12) channel signal sequence, wherein most source word-to-channel word conversions are parity preserving.

15 Fig. 1 shows an encoding device, which can be considered as a modification of the coding device 140, described in the above mentioned WO97/09718/A1 and applied in a recording device and a decoding and play back device described too in said document. Therefore, the contents of said document must be considered as inserted in the present specification.

20 The encoding device comprises converting means 1, arranged for converting n-bit source words into m-bit channel words, present in different coding states in a memory 2. The coding states are indicated by s bits. The input signals of the memory 2 are formed by a n-bit source word and a s-bit coding state number, indicating the current coding state where the relevant channel word can be found. The output signals of the memory 2 are formed by a m-bit channel word and a s-bit coding state number, indicating the next coding state, i.e. the state where the next channel word, corresponding with the next source word, can be found.
25 The next state number, supplied by the memory 2 is delivered to said memory via a buffer unit 3.

30 The m-bit channel words are supplied to a parallel-to-serial converter (P/S) 4 via a switching unit 5 described later on. The serial bit string from the parallel-to-serial converter 4 is supplied to a 1T-precoder 6, well known in the art. The output signal of the 1T-precoder 6 is applied to a control signal generator 7, which generates the control signal for the converting means 1, so as to insert after each block of p consecutive source words q dc-control source bits. The closed loop formed, formed by the converter means 1, the parallel-to-serial converter 4, the 1T-precoder 6 and the control signal generator 7 are well known in the

art, e.g. from US-A-5,477,222. The output signal of the device, supplied by the 1T-precoder is a RLL (run length limited) output signal.

The converting means 1 comprise a memory 2' for converting the q dc-control source bits into r dc-control channel bits, present in different coding states in the memory 2'.

- 5 In practice the memories 2 and 2' are integrated and form one memory 2, 2'. The coding states again are indicated by s bits. The input signals of the memory 2' are formed by the q dc-control source bits and a s -bit coding state number, indicating the current coding state where the relevant dc-control channel bits can be found. The output signals of the memory 2' are formed by r dc-control channel bits and a s -bit coding state number, indicating the next 10 coding state, i.e. the state where the next m -bit channel word, corresponding with the next n -bit source word, can be found. The next state number, supplied by the memory 2' is delivered to the memory 2 again via buffer unit 3.

15 The buffer unit 3 comprises a first and a second delay element 8 and 9 respectively and switching means 10 for passing either the next s state number bits from the memory 2 or the next s state number bits from the memory 2'. The switching means 10, as well as the switching means 5 are controlled by the timing unit (not indicated in the figure) of the device.

20 The invention will further been explained for an example wherein, each time after four ($p=4$) consecutive 8-bit source words ($n=8$) are converted into 15-bit channel words ($n=15$), a dc-control source bit ($q=1$) is converted into two dc-control channel bits ($r=2$) and wherein the memory 2 contains for each source word 4 possible channel words, arranged in state tables, indicated by a 2-bit state number ($s=2$) 1, 2, 3 or 4. When in the memory 2 a source word is converted into a channel word, the state number for the next conversion is read out too and supplied via delay element 8 and the switching means 10 with 25 a conversion clock delay to the input bus of the memory 2, so that the channel word for the next conversion is determined. The switching means 10 are in the position A in fig. 1. The channel word from the memory 2 is converted in a serial bitstring via the switching means 5 in the position A. After this process is repeated four times and, therefore, 4 consecutive source words are converted, from the bitstring of the obtained consecutive channel words and 30 via the 1T-precoder 6 and the control signal generator 7, a dc-control source bit "0" or "1" is generated and supplied to the memory 2'. As also the dc-control channel bits in the memory are dependent of the state number, the state number read out together with the last channel words indicates the state of the dc-control bit conversion. Therefore, the dc-control channel bits from memory 2 are supplied via delay element 8 and switching means 10 in the position

B to memory 2' too. Based on the dc-control source bit and the respective state number the dc-control channel bits are read out, together with the state number of the next source word conversion. The latter state number is supplied again to memory 2 via delay element 9, introducing a conversion clock delay, and the switching means 10 in the position B. The dc-
5 control channel bits are supplied to the parallel-to-serial converter 4 via the switching means 5 in the position B. Then, again 4 consecutive source words are converted into 4 corresponding channel words, whereafter again a dc-control source word is converted into a dc-control channel word. The result is that constantly the source words are aligned with the corresponding channel bits, so that, when during recording of the channel words on a carrier
10 or during reproducing from said carrier an error occurs, this error is restricted to only the source word, obtained after conversion of the channel word into said source during reproduction, and is not propagated to other source words reproduced.

An example of a dc-control bit conversion as registered in memory 2' is indicated in fig. 2. When a channel words ends with "1", the next state is state 1. Although
15 depending on this state and the dc-control source bit "0" or "1" the dc-control channel bits would be determined, the (d,k) sequence constraint with d=2 requires at least two zero's after an one, so that in both cases the dc-control channel bits will be "00". Depending on the dc-control source bit the next state (2 or 3 in fig. 2) is read out. Because in both cases there is no parity difference in the dc-control channel bits, such a parity difference must be made on
20 another way. To make a parity difference between the situations where the dc-control source bits are "0" or "1", according to the invention inverting means 11 are provided to convert an uneven number of source bits, preferably only one bit of the next source word. This bit-inverting control signal for the inverting means 11 is supplied by the memory 2' in response to a dc-control source bit "1" in state 1. When a channel word ends with two to eight zero's,
25 the dc-control channel bits can be found in states 2 or 3. In each of these states the dc-control channel bits have different parity dependent on the dc-control source bit. Therefore no source bits are inverted. When a channel word ends with "10", the dc-control channel bits can be found in state 4. Although not absolute necessary in view of the d=2 constraint, in this case, independent of the dc-control source bit the dc-control channel bits are "00", while the next
30 conversion must be found in states 2 and 3 respectively. Again, the difference between the situations where the dc-control source bit is "0" and "1" can be made by generating, in case the latter dc-control source bit is "1", a bit inverting control signal to invert a bit of the next source word. When a channel word ends with nine, ten or eleven zero's, the dc-control channel bits can also be found in state 4. In this case, independent of the dc-control source bit

the dc-control channel bits are "01 and 10" respectively, while the next conversion now must be found in states 1 and 4 respectively. As the latter dc-control channel bits have the same parity, the difference between the situations where the dc-control source bit is "0" and "1" can again be made by generating, in case the latter dc-control source bit is "1", a bit inverting control signal to invert a bit of the next source word. By the parity preserving property of the (d,k) code, a sign inversion of the outgoing bitstream during reproduction will occur. This, however, can be corrected easily because the combination of the dc-control channel bits and the last state number is unique.

The alignment of source words and channel words can be applied to several (d,k) codes. In the above bit sequence d=2. From WO97/09718/A1 a (2,14) bitsequence is known, however, without any parity preserving guarantee. By applying the invention it is possible to guarantee parity preserving in combination with alignment of source words and channel words. An example of such a code is given in figs. 3A-3H, which figure shows a (2,14) parity preserving code. As it is advantageous to restrict the k constraint as much as possible and to realize state tables, wherein multiple used channel words refer to a same source word as much as possible, a (2,13) parity preserving code has been found. This code is indicated in figs. 4A-4H. When identical channel words refer to different source words and an error in the state number indication occurs, during reproduction the wrong source word is obtained and possibly the wrong state number for the next channel word-to source word conversion. This results in another type of error propagation. In the above (2,13) code these errors are strongly reduced. Even a (2,12) code was found, wherein most of the 1024 source-to-channel conversions are parity preserving. Such a code is indicated in figs. 5A-5H; in that code only 10 of the 4×2^8 conversions are not parity preserving.

CLAIMS:

1. Device for encoding a stream of databits of a binary source signal into a stream of databits of a binary channel signal, wherein the bitstream of the source signal is divided into n-bit source words, which device comprises converting means adapted to convert a block of p consecutive n-bit source words into a corresponding block of p consecutive m-bit channel words, where p, n, m are integers and $m > n \geq 1$, the converting means comprising memory means which contain for each n-bit source word a number of m-bit channel words, arranged in coding states, and a corresponding state number, indicating the coding state for a next m-bit channel word, characterized in that the conversion for at least most of the n-bit source words is parity preserving and/or parity inverting, and that after each block of source words q dc-control sourcebits are added, which dc-control sourcebits are converted into r dc-control channelbits, independent of the conversion of a following source word, where q and r are integers.
2. Device for encoding a stream of databits of a binary source signal into a stream of databits of a binary channel signal, wherein the bitstream of the source signal is divided into n-bit source words, which device comprises converting means adapted to convert a block of p consecutive n-bit source words into a corresponding block of p consecutive m-bit channel words, where p, n, m are integers and $m > n \geq 1$, the converting means comprising memory means which contain for each n-bit source word a number of m-bit channel words, arranged in coding states, and a corresponding state number, indicating the coding state for a next m-bit channel word, characterized in that the conversion for at least most of the n-bit source words is parity preserving and/or parity inverting, and that after each block of source words q dc-control sourcebits are added, which dc-control sourcebits together with only a following n-bit source word is converted into a $(r+m)$ -bit channelword, where q and r are integers.
3. Device according to claim 1 or 2, characterized in that the channel output signal sequence supplied by the converting means is fed to a precoder to determine a RLL

(run length limited) output signal, which signal is supplied to a control signal generator to derive the dc-control bits.

4. Device according to any one of the claims 1-3, characterized in that the
5 memory means further contain for each q dc-control source bits and for each state number, r dc-control channel bits and a corresponding state number, indicating the memory location for a next m-bit channel word .

5. Device according to any one of the preceding claims, characterized in that
10 n=8, m=15, q=1 and r=2, while p is chosen dependent on the desired dc-suppression.

6. Device according to any one of the preceding claims, characterized in that the
device comprises inverting means, which, depending on a last preceding channelword, the
state number read out together with said last preceding channelword and on the dc-control
15 channel bits, can provide for inversion of an odd number of bits of a following source word.

7. Device according to any one of the preceding claims, characterized in that
multiple used channel words in the coding states refer substantially to a same source word.

20 8. Memory means with coding states for application in a device according to any
one of the preceding claims, characterized by 15-bit channel words in a parity preserving
(2,14) sequence.

9. Memory means with coding states for application in a device according to any
25 one of the preceding claims, characterized by 15-bit channel words in a parity preserving
(2,13) sequence.

10. Memory means with coding states for application in a device according to any
one of the preceding claims, characterized by 15-bit channel words in a (2,12) sequence,
30 while most of the 1024 source-to-channel conversions are parity preserving.

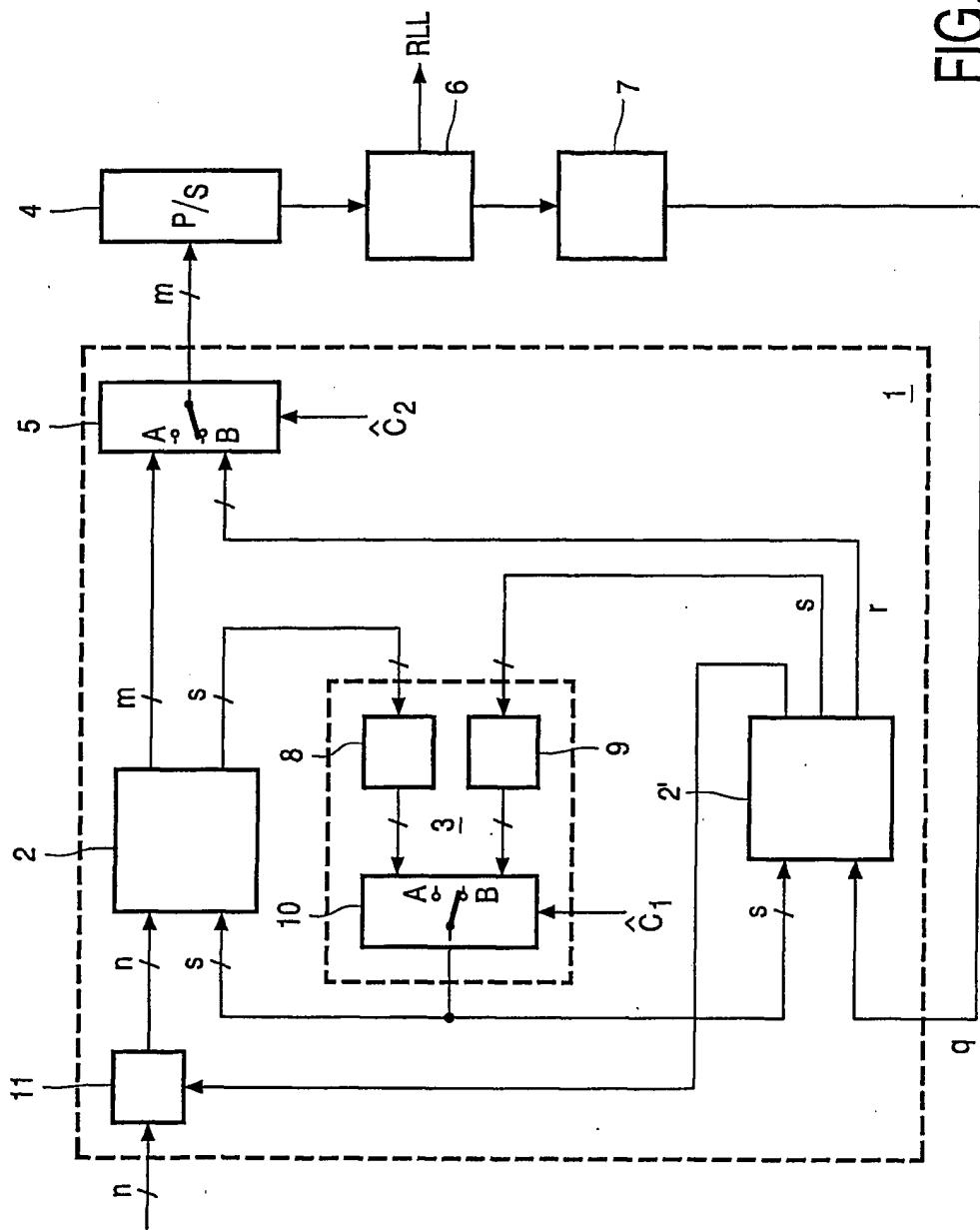
11. Device for recording information, which device comprises an encoding device
according to any one of the claims 1-7 for converting a series of channel words representing

the information into a modulated signal and means for recording an information pattern corresponding to said modulated signal on a record carrier.

12. Record carrier on which a modulated signal is recorded, said signal comprising a series of channel words, obtained by encoding source words according to any one of the claims 1-7.
13. Device for decoding channel words into source words comprising converting means with memory means containing the same coding states as the memory means in claim 10 or 2, which coding states are read out inversely.
14. Device for playing back comprising a reading arrangement for reading a record carrier according to claim 12 and a decoding device according to claim 13.

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FIG. 1



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The diagram illustrates a state transition table with two labels: 'in' and 'out'. The 'in' label is positioned above the first column of the table, and the 'out' label is positioned above the last column. The table has five columns: channel word, state, dc control source bit, dc control channel bit, and inverter signal.

channel word	state	dc control source bit	dc control channel bit	inverter signal
xxxxxx1.....x1	1	0	0	0
" "	1	1	0	1
xxxxx1(.....)00	2	0	0	0
" "	2	1	1	0
" "	3	0	0	3
" "	3	1	0	1
xxxxxx1.....x10	4	0	0	0
" "	4	1	0	3
xx1(..)00000000	4	0	1	1
" "	4	1	1	0

FIG. 2

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0 000100010010001
1 00010000000010001
2 00010000000010001
3 00010000000010001
4 00100100010001001
5 00001000010001001
6 00001000010001001
7 00010000010010001
8 00010000100010001
9 0001000100010001
10 0001000100010001
11 0001000100010001
12 001000010010001
13 0001000100010001
14 0001000100010001
15 0001000100010001
16 0001000100010001
17 0010000100010001
18 0001000100010001
19 0001000100010001
20 001000100010001
21 0001000100010001
22 0001000100010001
23 001000100010001
24 001000100010001
25 0001000000100100
26 0010000000100100
27 001000100010001
28 0010000010001000
29 0010001000100001
30 0010001000100001
31 0010000010010000

FIG. 3A

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FIG. 3B

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FIG. 3C

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FIG. 3D

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FIG. 3E

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3E
EIG

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192	00000100000100000	2	001000001000000	3	0100000100100100	1	1
193	0000010000010001	1	001000010000100	3	0100001000100000	3	2
194	0000010000010001	1	0010000100001000	3	0100001000100000	3	2
195	0000010000100000	2	001000010000000	3	010001000100100	3	1
196	000001000100001	1	001000010010000	3	010001000001000	3	2
197	00000100000000	2	001000100000000	3	0100010001000100	3	1
198	000000010000001	1	001000100100100	3	010001001001000	3	1
199	000001001000001	1	00100010001000	3	010001000001000	3	1
200	000001000001001	1	001000100001000	3	010001000010000	3	1
201	000000010000001	1	001001000100100	3	0100010001000100	3	1
202	000000100000001	1	0010010001000100	3	0100010001000100	3	1
203	000001000010001	1	001000100010000	3	010001000010000	3	1
204	000001000000001	1	0010010001001000	3	0100010001001000	3	1
205	0000010000100001	1	0010001000100000	3	0100010001000000	3	1
206	0000010000100001	1	0010001000100000	3	0100010001000000	3	1
207	0000010001000101	1	10000000000010	4	0100010001000010	3	1
208	0000010001000001	1	001001000010000	3	000000100010010	4	1
209	000001000000001	1	100000010010010	4	0100010001000100	3	1
210	0000010001001001	1	1000000100010010	4	0100010001000100	3	1
211	000000000000010	4	001001000010000	3	0000001000000010	4	1
212	000000000010010	4	10000001000100	4	0000001000000010	4	1
213	000000000010010	4	001001000010000	3	0000001000000000	4	1
214	000000000010010	4	00100010000000	3	0000001000000000	4	1
215	000000000010010	4	10000001000000	4	0000001000000000	4	1
216	000000001000010	4	1000001000010010	4	0000010000000010	4	1
217	000000100100010	4	1000000000100010	4	0000001000010010	4	1
218	000000100000000	4	1000000000100010	4	00000010000100010	4	1
219	000000010000010	4	10000001000010	4	000010010010010	4	1
220	0000001000010010	4	1000000000100010	4	0000100000000000	4	1
221	0000000100000010	4	1000000000100010	4	0001000000000010	4	1
222	0000001000000010	4	10001000000000	4	000100010010010	4	1
223	00000010000100010	4	1000000000100010	4	0000001000000010	4	1

FIG. 3G

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FIG. 3H

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FIG. 4A

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FIG. 4B

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FIG. 4C

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96	001000100100100	3	001000100100100	001000100100100	3
97	001001000000100	3	001001000000100	001001000000100	3
98	0010010000001000	3	0010010000001000	0010010000001000	3
99	001001000100100	3	001001000100100	001001000100100	3
100	001001000010000	3	001001000010000	001001000010000	3
101	001001001000100	3	001001001000100	001001001000100	3
102	001001001001000	3	001001001001000	001001001001000	3
103	0010010010001000	3	0010010010001000	0010010010001000	3
104	001001001000000	3	001001001000000	001001001000000	3
105	000100000000010	4	100000010000000	2	000100000000010
106	000100010010010	4	100000100000000	2	000100010010010
107	00010000010010	4	100000010000100	2	00010000010010
108	000100100010010	4	100000100100100	2	000100100100100
109	00010000100010	4	10000010001000	2	00010000100010
110	000100001000010	4	10000010000100	2	000100001000010
111	000100100100010	4	100000100100010	2	000100100100010
112	000100010000010	4	100000010000010	2	000100010000010
113	00100000000010	4	00100000000010	4	010010001000100
114	001000010010010	4	00100010010010	4	01001000100100
115	00010010000010	4	100000010000100	2	000100010000010
116	001000100010010	4	001000100010010	4	0100000000100
117	00100000010010	4	00100000010010	4	01000000010010
118	001000000100010	4	001000000100010	4	010000000100010
119	001000100100010	4	001000100100010	4	010000000100010
120	00100100000000	4	00100100000000	4	010000000100000
121	00100001000010	4	00100001000010	4	010000000100000
122	001000010000010	4	001000010000010	4	010000000100000
123	001001000010010	4	001001000010010	4	010000000100000
124	001000100000010	4	001000100000010	4	010000000100000
125	001001000100010	4	001001000100010	4	010000000100000
126	0010010001000010	4	0010010001000010	4	010000000100000
127	001000100000010	4	001000100000010	4	010000000100000

FIG. 4D

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FIG. 4E

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FIG. 4F

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FIG. 4G

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FIG. 4H

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FIG. 5A

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FIG. 5B

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FIG. 5C

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FIG. 5D

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FIG. 5E

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FIG. 5F

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FIG. 5G

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1 3
2 2
3 1
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FIG. 5H

INTERNATIONAL SEARCH REPORT

Int'l Application No
PCT/EP 01/05505

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M5/14 G11B20/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M G11B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 151 699 A (MORIYAMA YOSHIAKI) 29 September 1992 (1992-09-29) abstract figures 2,3 column 3, line 49 -column 4, line 45 ---	1,3, 11-14
Y	WO 99 33183 A (SONY CORP ;KONINKL PHILIPS ELECTRONICS NV (NL)) 1 July 1999 (1999-07-01) the whole document ---	1,3, 11-14
A	WO 99 35747 A (KAHLMAN JOSEPHUS A H M ;KONINKL PHILIPS ELECTRONICS NV (NL); PHILI) 15 July 1999 (1999-07-15) page 2, line 3 -page 3, line 18 page 4, line 15 -page 8, line 19 figure 1 ---	1-3, 11-14 -/-

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Patent family members are listed in annex.

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Date of the actual completion of the International search

21 September 2001

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax (+31-70) 340-3016

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INTERNATIONAL SEARCH REPORT

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